

App. Serial No. 10/538,217
Docket No.: NI.021418 US

RECEIVED
CENTRAL FAX CENTER

APR 30 2007

In the Claims:

Please amend claims 1, 3 and 9 and add new claims 11-16 as indicated below.
This listing of claims replaces all prior versions.

1. (Currently Amended) A method of manufacturing a trench gate semiconductor device comprising the steps of: providing a silicon device body having a first major surface, the silicon device body having a drain region of a first conductivity type and a body region over the drain region; forming a trench extending downwards into the silicon device body from the first major surface, the trench having sidewalls and a base; etching the silicon at the base of the trench to form porous silicon at the base of the trench; and thermally ~~oxidising~~ oxidizing the device to ~~oxidise~~ oxidize the porous silicon at the bottom of the trench to form a plug at the base of the trench; and depositing conductive material within the trench to form a gate.
2. (Original) A method according to claim 1 further comprising, after the step of etching the trench, the step of lining the side walls of the trench with dielectric liner for preventing the side walls becoming porous during the step of forming porous silicon at the bottom of the trench.
3. (Currently Amended) A method according to claim 1 wherein the step of ~~oxidising~~ oxidizing the device forms sidewall oxide on the sidewalls of the trench, the method further comprising the steps of etching away the oxide formed on the side wall oxide and of forming the gate oxide by thermal oxidation on the side wall before the step of depositing conductive material within the trench to form a gate.
4. (Previously Presented) A method according to claim 1 wherein the step of forming the trench includes providing a mask on the first major surface defining an opening and etching the trench extending downwards from the first major surface through the opening.

App. Serial No. 10/538,217
Docket No.: NL021418 US

5. (Original) A method according to claim 4 wherein the mask is an oxide hard mask.
6. (Original) A method according to claim 4 wherein the step of etching the silicon at the bottom of the trench to form porous silicon includes dry-etching the bottom of the trench through the same mask used to define the trench.
7. (Previously Presented) A method according to claim 1 further comprising depositing a silicon plug in the trench wherein the step of etching the silicon at the bottom of the trench includes etching the silicon plug.
8. (Previously Presented) A method according to claim 1 further comprising forming a source implant of first conductivity type at the first major surface adjacent to the trench and forming source, gate and drain electrodes attached to the source implant, the gate and the drain region at the bottom of the trench respectively to complete the trench gate semiconductor device.
9. (Currently Amended) A trench MOSFET comprising: a drain region of first conductivity type; a body region over the drain region; a trench extending from a first major surface through the body region; source regions of the first conductivity type laterally adjacent to the trench at the first major surface; thermal gate oxide on the side walls of the trench; a gate electrode in the trench insulated from the body region by the gate oxide; characterised by a thick oxide plug formed of ~~oxidised~~ oxidized porous silicon at the base of the trench extending into the drain region.
10. (Original) A trench MOSFET according to claim 9 wherein the body region is of second conductivity type opposite to the first conductivity type.
11. (New) A method of manufacturing a trench gate semiconductor device, the method comprising:

App. Serial No. 10/538,217
Docket No.: NL021418 US

providing a silicon device body having a first major surface, the silicon device body having a drain region of a first conductivity type and a body region over the drain region;

forming a trench extending downwards into the silicon device body from the first major surface, the trench having sidewalls and a base;

etching the silicon at the base of the trench to form porous silicon at the base of the trench;

thermally oxidizing the device to oxidize the porous silicon at the base of the trench to form a plug at the base of the trench, wherein thermally oxidizing the device forms sidewall oxide on the sidewalls of the trench; and

depositing conductive material within the trench to form a gate.

12. (New) The method of claim 11, further comprising etching away the sidewall oxide and forming a gate oxide by thermal oxidation on the sidewalls of the trench before depositing conductive material within the trench to form a gate.

13. (New) The method of claim 11, wherein forming the trench includes providing a mask having an opening and on the first major surface and etching through the opening.

14. (New) The method of claim 13, wherein the mask is an oxide hard mask.

15. (New) The method of claim 13, wherein etching the silicon at the base of the trench to form porous silicon includes dry-etching the base of the trench through the same mask used to define the trench.

16. (New) The method of claim 13, further comprising forming a source implant of the first conductivity type at the first major surface adjacent to the trench and forming source, gate and drain electrodes attached to the source implant, the gate and the drain region at the bottom of the trench respectively.

App. Serial No. 10/538,217
Docket No.: NL021418 US

In the Drawings:

Attached please find one Replacement Drawing Sheet, identified as Figures 3a-3b and Figure 4. The only change is the addition of the legend "Prior Art," to Figure 4. No other changes have been made to the Drawing Sheet.

Entry of this Replacement Drawing Sheet is respectfully requested.

Attachment: (1) Replacement Drawing Sheet